Claim Amendments:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. – 13. (Canceled)

14. (Previously Presented) An apparatus comprising:

semiconductor substrate having an input output (IO) ring, the IO ring having a bond pad portion and an active buffer portion;

the bond pad portion including:

a first bond pad;

a second set of bond pads having one or more bond pads;

a third bond pad, wherein the second set of bond pads is immediately adjacent to the first and third bond pads; and

a first conductive trace coupling the first bond pad to the third bond pad;

a second conductive trace coupling the first bond pad to a power buffer; and

a third conductive trace coupling one of the bond pads of the second set of bond pads to a signal buffer.

15. (Previously Presented) The apparatus of claim 14, wherein the first bond pad and the third bond pad are to be coupled to a fixed voltage source.

16. (Original) The apparatus of claim 15, wherein the fixed voltage source is one of Vdd and Vss.

17. (Previously Presented) The apparatus of claim 14, further comprising:

a package substrate having a power portion, wherein the power portion is to provide a fixed voltage;

a first bond wire connected to the first bond pad and the power portion; and

a second bond wire connected to the third bond pad and the power portion.

18. (Original) The apparatus of claim 17 further comprising exactly one of the first bond pad and the third bond pad being connected to the active buffer portion of the IO ring.

19. (Original) The apparatus of claim 14, wherein the second set of bond pads includes one bond pad.

20. (Previously Presented) The apparatus of claim 14, wherein the second set of bond pads includes more than one bond pad.

21. (Previously Presented) The apparatus of claim 14, wherein the signal buffer is an input buffer.

22. (Previously Presented) The apparatus of claim 14, wherein the signal buffer is an output buffer.

23. (Previously Presented) The apparatus of claim 14, wherein the signal buffer is a bidirectional buffer.

24. (Previously Presented) An apparatus comprising:

a semiconductor substrate including

a signal buffer;

a power buffer immediately adjacent to the signal buffer;

a first bond pad coupled to the power buffer;

a second bond pad coupled to the power buffer;

a third bond pad coupled to the signal buffer, wherein the third bond pad is immediately adjacent to the first and the second bond pad.

25. (Previously Presented) The apparatus of claim 24, wherein the second bond pad is coupled to the first bond pad in a bond pad portion of the apparatus.